Remarks

As stated above, the applicants appreciate the Examiner's thorough examination of the subject application and request reexamination and reconsideration of the subject application in view of the preceding amendments and the following remarks.

Concerning Item 1 of the Subject Action, the Examiner objects to claim 35, requesting that the claim be amended to read "...wherein the one or more instructions further comprise instructions...". Accordingly, the applicant has amended claim 35 pursuant to the Examiner's request.

Concerning Item 2 of the subject action, the Examiner rejects claims 1-6, 9-12, 15-19, 22-26 and 29-33, under 35 USC §102(b), based on the teachings of Anderson (U.S. Patent No. 5,898,869; hereinafter Anderson).

Applicants claim (in currently amended claim 1):

> 1. A system comprising: (a) a core processing circuit; and (b) a host processing system coupled to the core processing circuit through a host bridge, the host processing system comprising: (b1) logic to maintain the core processing circuit in a reset state during power up of the core processing circuit; and (b2) logic to load a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions to initialize the core processing circuit upon release from the reset state. *Emphasis Added.*

Applicants claim (in currently amended claim 9):

> 9. A method comprising: (a) having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit; and (b) loading a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions from a system memory coupled to the core processing circuit through a host bridge of a host processing system. *Emphasis Added.*

Applicants claim (in currently amended claim 15):

> 15. A method comprising: (a) having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit; and (b) loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit, the instructions comprising one or more instructions to initialize the core

processing circuit upon release of the core processing circuit from the reset state. *Emphasis Added.*

Applicants claim (in currently amended claim 22):

> 22. An article comprising: (a) a storage medium comprising machine-readable instructions encoded there on for: (b) having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit; and (c) loading a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions from a system memory coupled to the core processing circuit through a host bridge of a host processing system. *Emphasis Added.*

Applicants claim (in currently amended 29):

> 29. An article comprising: (a) a storage medium comprising machine-readable instructions encoded there on for: (b) having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit; and (c) loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit, the instructions comprising one or more instructions to initialize the core processing circuit upon release from the reset state. *Emphasis Added.*

Applicants respectfully assert that Anderson fails to disclose element (b1) of applicants' claim 1, "[the host processing system comprising] logic to maintain the core processing circuit in a reset state during power up of the core processing circuit". Further, applicants respectfully assert that Anderson fails to disclose element (a) of applicants' claim 9, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit". Additionally, applicants respectfully assert that Anderson fails to disclose element (a) of applicants' claim 15, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit". Further, applicants respectfully assert that Anderson fails to disclose element (b) of applicants' claim 22, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit". Finally, applicants respectfully assert that Anderson fails to disclose element (b) of applicants' claim 29, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit".

Accordingly, applicants respectfully assert that Anderson is not a proper basis for a 35 USC §102(b) rejection, as the reference fails to disclose each and every element of the applicants' claimed invention.

Concerning the logic to place the core processing circuit in a reset state claimed by the applicants, applicants disclose that:

> the host processing system may cause the core processing circuit 26 to be powered up while maintaining the core processing circuit 26 in a reset state. For example, the host processing system may initiate one or more write bus transactions on the data bus 18 to control registers defined in the memory 30 which control the power state of the peripheral controller 20. Alternatively, the host processing system may assert signals on one or more pins (not shown) to apply power to the peripheral controller 20. *See the subject application, paragraph 31, emphasis added.*

Further, applicants disclose that:

> Once the peripheral controller 20 is powered, the host processing system may maintain the core processing circuit 26 in a reset state by, for example, initiating one or more write bus transactions on the data bus 18 to control registers which control the reset state of the core processing circuit 26. Alternatively, the host processing system may assert signals on one or more pins (not shown) of the peripheral controller 20 to maintain the core processing circuit in a reset state. *See the subject application, paragraph 32, emphasis added.*

Accordingly, applicants' core processing circuit is controlled by the host processing system, wherein controlling includes causing "the core processing circuit 26 to be powered up while maintaining the core processing circuit 26 in a reset state" and maintaining "the core processing circuit 26 in a reset state". Additionally, "[o]nce the peripheral controller 20 is powered, the host processing system may maintain the core processing circuit 26 in a reset state by, for example, initiating one or more write bus transactions on the data bus 18 to control registers which control the reset state of the core processing circuit 26".

Applicants respectfully assert that Anderson fails to disclose such a system. Specifically, concerning processor 31 of the PCMCIA card (which the Examiner asserts is synonymous to the applicants' core processing circuit), and the manner in which processor 31 is reset, Anderson discloses that:

> a flip-flop 55 controls the resetting, and accordingly booting, of processor 31. In the current embodiment, flip-flop 55 is implemented within the programmable logic of PLD 33, but could be otherwise implemented in, e.g., discrete logic. Flip-flop 55 is of a D-type and has a Q output 61, a D input 67, a clock input 65 and an asynchronous clear ("CL") input 63. D input 67 is tied to a logic 1 state; Q output 61 is coupled to a RESET* 58 input of processor 31 by VRST* line 57 ("VRST*" is an active low signal for resetting processor 31); clock input 63 is coupled to the CSO output of PCMCIA interface 17 by a START* line 51 ("START*" is an active low signal for starting processor 31); and clear input 53 is coupled to the HRESET* output of PCMCIA interface 17 by SRST* line 53 ("SRST*" is an active low system reset line for resetting processor 31 and other resettable circuitry on PCMCIA card 13, e.g., PLD 33 and buffers 35). *See Anderson, column 6, lines 33-44.*
>
> To briefly summarize, operationally, when PCMCIA card 13 is reset through a software or hardware reset, HRESET* is asserted causing flip-flop 55 to clear, lowering its Q output 61, thereby causing processor 31 to enter a reset state. Processor 31 is maintained in reset by Q output 61 of flip-flop 55 while dual-ported memory 39 (e.g., FIG. 1) is loaded with boot code for processor 31. Thereafter, an access by host 11 to PCMCIA card 13 within an address range corresponding to CSO causes the assertion of START* line 51 and the latching of Q output 61 to a logic high state. Processor 31 then leaves its reset state and boots. In the current example, wherein processor 31 is an Intel brand 80C186EC processor, booting begins at memory location FFFF0H, and dual-ported memory 39 is mapped therein such that booting occurs therefrom. *See Anderson, column 6, lines 1-15.*

Accordingly, applicants respectfully assert that Anderson is not a proper basis for a 35 USC §102(b) rejection, as the reference fails to disclose each and every element of applicants' currently-amended claims 1, 9, 15, 22 and 29. Therefore, the applicants respectfully assert that independent claims 1, 9, 15, 22 and 29 are patentable over the cited reference.

Further, as dependent claims 2-8 depend (either directly or indirectly) upon independent claim 1, applicants respectfully assert that claims 2-8 are also patentable over the cited reference. Additionally, as dependent claims 10-14 depend (either directly or indirectly) upon independent claim 9, applicants respectfully assert that claims 10-14 are also patentable over the cited reference. Further, as dependent claims 16-21 depend (either directly or indirectly) upon independent claim 15, applicants respectfully assert that claims 16-21 are also patentable over the cited reference. Additionally, as dependent claims 23-28 depend (either directly or indirectly) upon independent claim 22, applicants respectfully assert that claims 23-28 are also

patentable over the cited reference. Finally, as dependent claims 30-35 depend (either directly or indirectly) upon independent claim 29, applicants respectfully assert that claims 30-35 are also patentable over the cited reference.

Concerning Item 3 of the subject action, the Examiner rejects claims 7, 13, 20, 27 and 34, under 35 USC §103(a), based on the teachings of Anderson.

For the reasons discussed above, the applicants respectfully assert that Anderson fails to disclose element (b1) of applicants' claim 1, "[the host processing system comprising] logic to maintain the core processing circuit in a reset state during power up of the core processing circuit". Further, applicants respectfully assert that Anderson fails to disclose element (a) of applicants' claim 9, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit". Additionally, applicants respectfully assert that Anderson fails to disclose element (a) of applicants' claim 15, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit". Further, applicants respectfully assert that Anderson fails to disclose element (b) of applicants' claim 22, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit". Finally, applicants respectfully assert that Anderson fails to disclose element (b) of applicants' claim 29, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit".

As dependent claim 7 depends (either directly or indirectly) upon independent claim 1, dependent claim 13 depends (either directly or indirectly) upon independent 9, dependent claim 20 depends (either directly or indirectly) upon independent claim 15, dependent claim 27 depends (either directly or indirectly) upon independent 22, and dependent claim 34 depends (either directly or indirectly) upon independent 29, the applicants respectfully assert that claims 7, 13, 20, 27 and 34 are also patentable over the cited reference.

Concerning Item 3 of the subject action, the Examiner further rejects claims 8, 14, 21, 28 and 35, under 35 USC §103(a), based on the combination of the teachings of Anderson, and Klein (U.S. Patent No. 6,226,224; hereinafter Klein).

For the reasons discussed above, the applicants respectfully assert that Anderson fails to disclose element (b1) of applicants' claim 1, "[the host processing system comprising] logic to

maintain the core processing circuit in a reset state during power up of the core processing circuit". Further, applicants respectfully assert that Anderson fails to disclose element (a) of applicants' claim 9, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit". Additionally, applicants respectfully assert that Anderson fails to disclose element (a) of applicants' claim 15, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit". Further, applicants respectfully assert that Anderson fails to disclose element (b) of applicants' claim 22, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit". Finally, applicants respectfully assert that Anderson fails to disclose element (b) of applicants' claim 29, namely "having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit".

As dependent claim 8 depends (either directly or indirectly) upon independent claim 1, dependent claim 14 depends (either directly or indirectly) upon independent 9, dependent claim 21 depends (either directly or indirectly) upon independent claim 15, dependent claim 28 depends (either directly or indirectly) upon independent 22, and dependent claim 35 depends (either directly or indirectly) upon independent 29, the applicants respectfully assert that claims 8, 14, 21, 28 and 35 are also patentable over the cited reference.

No new matter has been added by these amendments. While the applicants respectfully assert that the subject application is now in condition for allowance, the Examiner is invited to telephone applicants' attorney (603-668-6560) to facilitate prosecution of this application. Please apply any charges or credits to deposit account 50-2121.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 31 day of May, 2005.

Chris Hammond
Name

Chris Hammond
Signature